Listing of Claims:

1-18. (canceled).

19. (currently amended) A network processing device, comprising:

an ingress circuit configured to process packets received over a network;

an egress circuit configured to process packets for sending over the network;

a reconfigurable switch fabric for <u>receiving</u> ~~transferring~~ scrambled data <u>at a first</u> ~~between~~ ~~a plurality of~~ switch fabric ~~ports~~ <u>port and retransmitting the scrambled data, respectively, at at</u> <u>least one switch fabric port selected from a second plurality of switch fabric ports</u>;

<u>a backplane coupled to the switch fabric ports;</u> and

a first scrambler circuit configured to scramble a first parallel array of packet bits received from the ingress circuit into a first array of scrambled output bits for <u>sending over the</u> <u>backplane to the first switch fabric port for</u> switching across the switch fabric <u>and retransmission</u> <u>over the backplane from one of the second plurality of switch fabric ports</u> towards the egress circuit.

20. (previously presented) A network processing device according to claim 19 including a first new seed register for storing the first array of scrambled output bits and supplying the first array of scrambled output bits to the first scrambler circuit for applying to a second parallel array of bits received from the ingress circuit.

21. (previously presented) A network processing device according to claim 20, further comprising a second scrambler circuit and a second new seed register located in the egress circuit for scrambling the packets processed by the egress circuit before sending those packets over the network.

22. (currently amended) A network processing device according to claim 20, further comprising a first de-scrambler circuit coupled to the egress circuit <u>and the backplane</u> and configured to receive scrambled data <u>over the backplane</u> from the switch fabric, the scrambled data comprising

the first array of scrambled output bits, and de-scramble the first array of scrambled output bits into a first array of descrambled packet bits.

23. (currently amended) A network processing device according to claim 22 including a first de-scrambler new seed register for storing the first array of de-scrambled packet bits and supplying the first array of de-scrambled ~~output~~ packet bits to the first de-scrambler circuit for applying to a second array of scrambled output bits received from the switch fabric.

24. (previously presented) A network processing device according to claim 23, further comprising a second de-scrambler circuit and a second de-scrambler new seed register located in the ingress circuit for descrambling arrays of scrambled bits received from the network.

25. (currently amended) A method for switching packet data between a plurality of network ports, comprising:

　　　　receiving packet data from a network;

　　　　scrambling a first parallel array of bits from the packet data into an array of first scrambled output bits;

　　　　~~transferring~~ transmitting the first scrambled output bits over a backplane to ~~through~~ a reconfigurable switch fabric;

　　　　retransmitting the first scrambled output bits over the backplane from the reconfigurable switch fabric; and

　　　　descrambling the first scrambled output bits after transferring the first scrambled output bits ~~through~~ from the reconfigurable switch fabric over the backplane.

26. (previously presented) A method according to claim 25 including storing the first scrambled output bits as new seed values for applying scramble polynomials to a second parallel array of bits from the packet data.

27. (previously presented) A method according to claim 26 including selecting the new seed values according to scramble polynomial values, a bit length of the parallel arrays of bits, and a position of the individual bits in the parallel arrays of input bits.

28. (previously presented) A method according to claim 26 including using the stored first scrambled output bits to apply a $1 + X(39) + X(58)$ scramble polynomial to each one of the second parallel array of input bits.

29. (currently amended) A method according to claim 25 wherein descrambling the first scrambled output bits comprises:

      receiving the first scrambled output bits;

      storing an array of previously de-scrambled output bits; and

      applying the array of previously de-scrambled output bits during descrambling of the first scrambled output bits to create first de-scrambled output bits.

30. (previously presented) A method according to claim 29 including storing the first de-scrambled output bits as new seed values for applying to a next group of scrambled output bits.